What is claimed is:

1. A transistor comprising:

a first and second source/drain region;

a body region located between the first and second source/drain regions, wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a praseodymium oxide dielectric layer on the surface portion of the body region; and

a gate on the praseodymium oxide dielectric layer.

2. The transistor of claim 1, wherein the surface portion of the body region is oriented in a (100) crystalline plane.

3. The transistor of claim 1, wherein the surface portion of the body region is oriented in a (111) crystalline plane.

4. The transistor of claim 1, wherein the praseodymium oxide dielectric layer is substantially amorphous.

5. The transistor of claim 1, wherein the praseodymium oxide dielectric layer is substantially without a silicon oxide.

6. The transistor of claim 1, wherein the praseodymium oxide dielectric layer provides a gate dielectric layer substantially without a silicide.

7. A transistor comprising:

a first and second source/drain region;

a body region located between the first and second source/drain regions, wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a Pr_2O_3 dielectric layer on the surface portion of the body region, wherein the Pr_2O_3 dielectric layer has a dielectric constant of about 31; and

a gate on the Pr_2O_3 dielectric layer.

8. The transistor of claim 7, wherein the surface portion of the body region is oriented in a (100) crystalline plane.

9. The transistor of claim 7, wherein the surface portion of the body region is oriented in a (111) crystalline plane.

10. The transistor of claim 7, wherein the Pr_2O_3 dielectric layer is substantially amorphous.

11. A transistor comprising:

a first and second source/drain region;

a body region located between the first and second source/drain regions, wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a Pr_2O_3 dielectric layer on the surface portion of the body region; and

a gate on the Pr_2O_3 dielectric layer;

the Pr_2O_3 dielectric layer formed by a process including:

evaporation depositing a praseodymium (Pr) metal layer on the body region;

oxidizing the Pr metal layer to form the Pr_2O_3 dielectric layer on the body region.

12. The transistor of claim 11, wherein evaporation depositing the Pr metal layer includes evaporation depositing by electron beam evaporation.

13. The transistor of claim 11, wherein oxidizing the Pr metal layer includes oxidizing using a krypton (Kr)/oxygen (O_2) mixed plasma process.

14. A transistor comprising:

a first and second source/drain region;

a body region located between the first and second source/drain regions;

a praseodymium oxide dielectric layer on the body region; and

a gate on the praseodymium oxide dielectric layer;

the praseodymium oxide dielectric layer formed by a process including:

evaporation depositing a praseodymium (Pr) metal layer on the body region;

oxidizing the Pr metal layer to form the praseodymium oxide dielectric layer on the body region.

15. The transistor of claim 14, wherein the praseodymium oxide dielectric layer has an equivalent oxide thickness of less than 2 nanometers.

16. The transistor of claim 14, wherein evaporation depositing the Pr metal layer includes evaporation depositing by electron beam evaporation and oxidizing the Pr metal layer includes oxidizing the Pr metal layer with atomic oxygen.

17. The transistor of claim 14, wherein the process for forming the praseodymium oxide dielectric layer includes forming the praseodymium oxide dielectric layer substantially without a silicon oxide.

18. The transistor of claim 14, wherein the process for forming the praseodymium oxide dielectric layer includes forming the praseodymium oxide dielectric layer substantially without a silicide.

19. A memory comprising:

a number of access transistors, each access transistor including:

a first and second source/drain region;

a body region located between the first and second source/drain regions,

wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a praseodymium oxide dielectric layer on the surface portion of the body region; and

a gate on the praseodymium oxide dielectric layer;

a number of wordlines coupled to a number of the gates of the number of access transistors;

a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors; and

a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors.

20. The memory of claim 19, wherein the praseodymium oxide dielectric layer exhibits a dielectric constant (k) of approximately 31.

21. The memory of claim 19, wherein the praseodymium oxide dielectric layer is substantially amorphous.

22. The memory of claim 19, wherein the praseodymium oxide dielectric layer provides a gate dielectric layer substantially without a silicon oxide and substantially without a silicide.

23. A memory comprising:

a number of access transistors, each access transistor including:

a first and second source/drain region;

a body region located between the first and second source/drain regions,

wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a praseodymium oxide dielectric layer on the surface portion of the body region, the praseodymium oxide dielectric layer having an equivalent oxide thickness less than 2 nanometers; and

a gate on the praseodymium oxide dielectric layer.

24. The memory of claim 23, wherein the praseodymium oxide dielectric layer provides a gate dielectric layer substantially without a silicon oxide.

25. The memory of claim 23, wherein the memory is a dynamic random access memory.

26. The memory of claim 23, wherein the memory is a flash memory.

27. An information handling device comprising:

a processor;

a memory device including:

a number of access transistors, each access transistor including:

a first and second source/drain region;

a body region located between the first and second source/drain regions, wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a praseodymium oxide dielectric layer on the surface portion of the body region; and

a gate on the praseodymium oxide dielectric layer;

a number of wordlines coupled to a number of the gates of the number of access transistors;

a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors; and

a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors; and

a system bus coupling the processor to the memory device.

28. The information handling device of claim 27, wherein the praseodymium oxide dielectric layer exhibits a dielectric constant (k) of approximately 31.

29. The information handling device of claim 27, wherein the praseodymium oxide dielectric layer is substantially amorphous.

30. The information handling device of claim 27, wherein the information handling includes a computer.

31. An information handling device comprising:

a processor;

a memory device including:

a number of access transistors, each access transistor including:

a first and second source/drain region;

a body region located between the first and second source/drain regions, wherein a surface portion of the body region has a surface roughness of approximately 0.6 nm;

a praseodymium oxide dielectric layer on the surface portion of the body region, the praseodymium oxide dielectric layer having an equivalent oxide thickness less than 2 nanometers; and

a gate on the praseodymium oxide dielectric layer; and

a system bus coupling the processor to the memory device.

32. The information handling device of claim 31, wherein the praseodymium oxide dielectric layer provides a gate dielectric layer substantially without a silicon oxide.

33. The information handling device of claim 31, wherein the memory device is a flash memory.

34. The information handling device of claim 31, wherein the information handling includes a computer.